**CURRENT DISTRIBUTION INTO BATTERY implementation using VERILOG HDL**

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**Aim: To divide the input current I into 4 parts i1,i2,i3,i4 based on certain inputs soc1,soc2,soc3,soc4.**

**i1,i2,i3,i4 and**  **soc1,soc2,soc3,soc4  are floating point numbersrepresented according to 32-bit single precision representation if IEEE 754.**

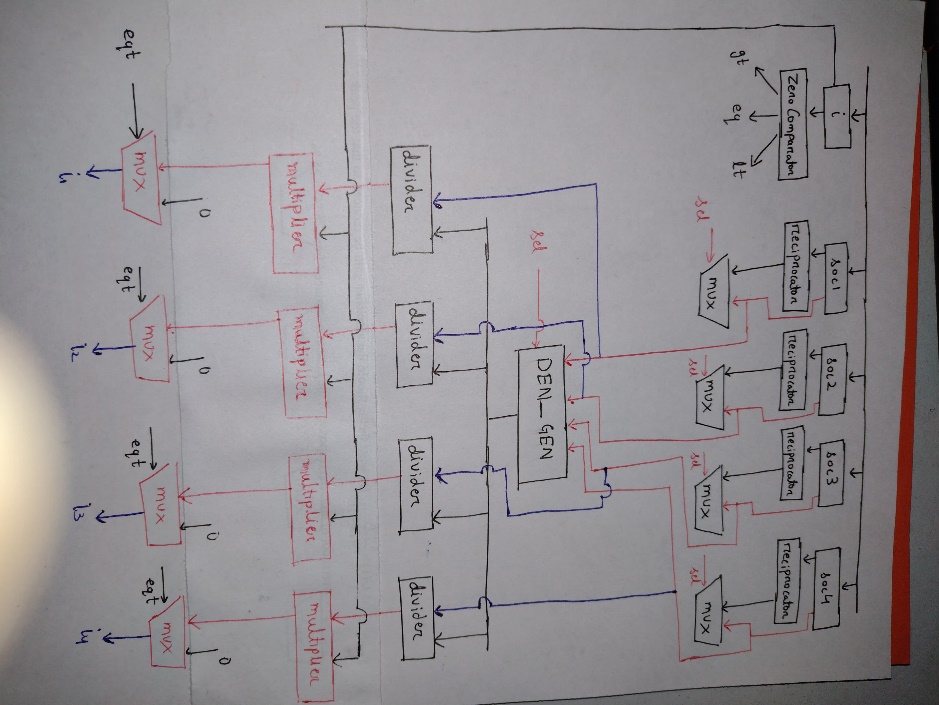
**Component Modules Used**

|  |  |  |
| --- | --- | --- |
| **SL. NO.** | **Module Name** | **Functionality** |
| **1** | **ZeroComparator** | **To check if input floating point number is equal, greater of less than zero.** |
| **2** | **Reciprocator** | **To calculate the reciprocal of a floating point number.** |
| **3** | **2-1 MUX** | **Selects one input out of two.** |
| **4** | **Divider** | **Divides two floating point number.** |
| **5** | **Multiplier** | **Multiplies two floating point number.** |
| **6** | **Adder** | **Adds 4 floating point number.** |
| **7** | **Den\_Gen** | **To generate the denominator in different cases.** |

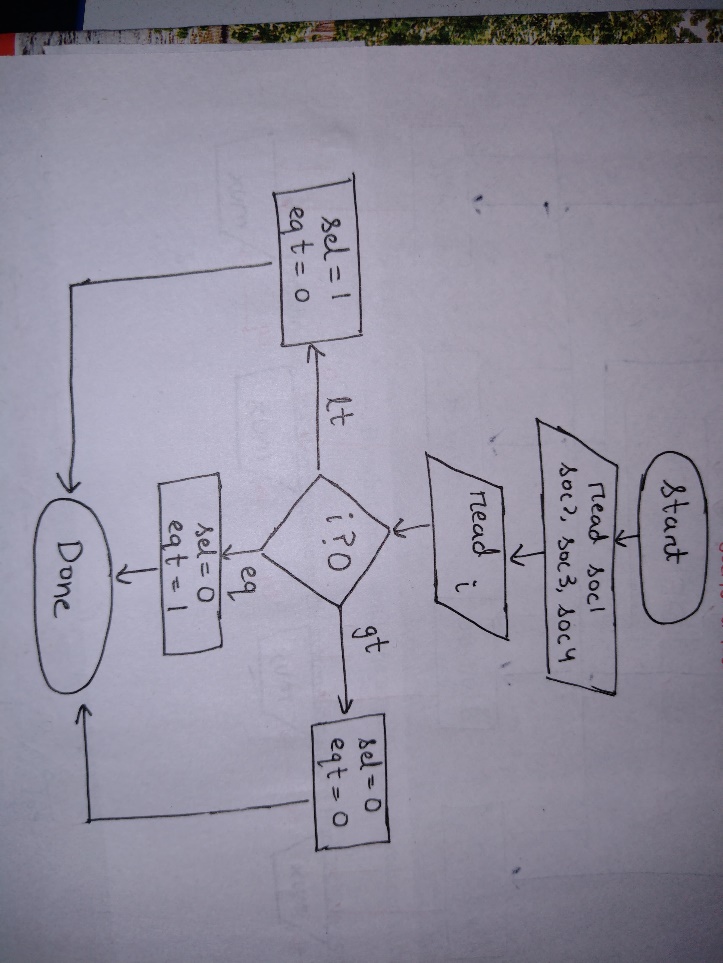
**Datapath: To process the input to generate the divided currents**

**Control Path: To control the signal and to ensures synchronous functioning of system.**

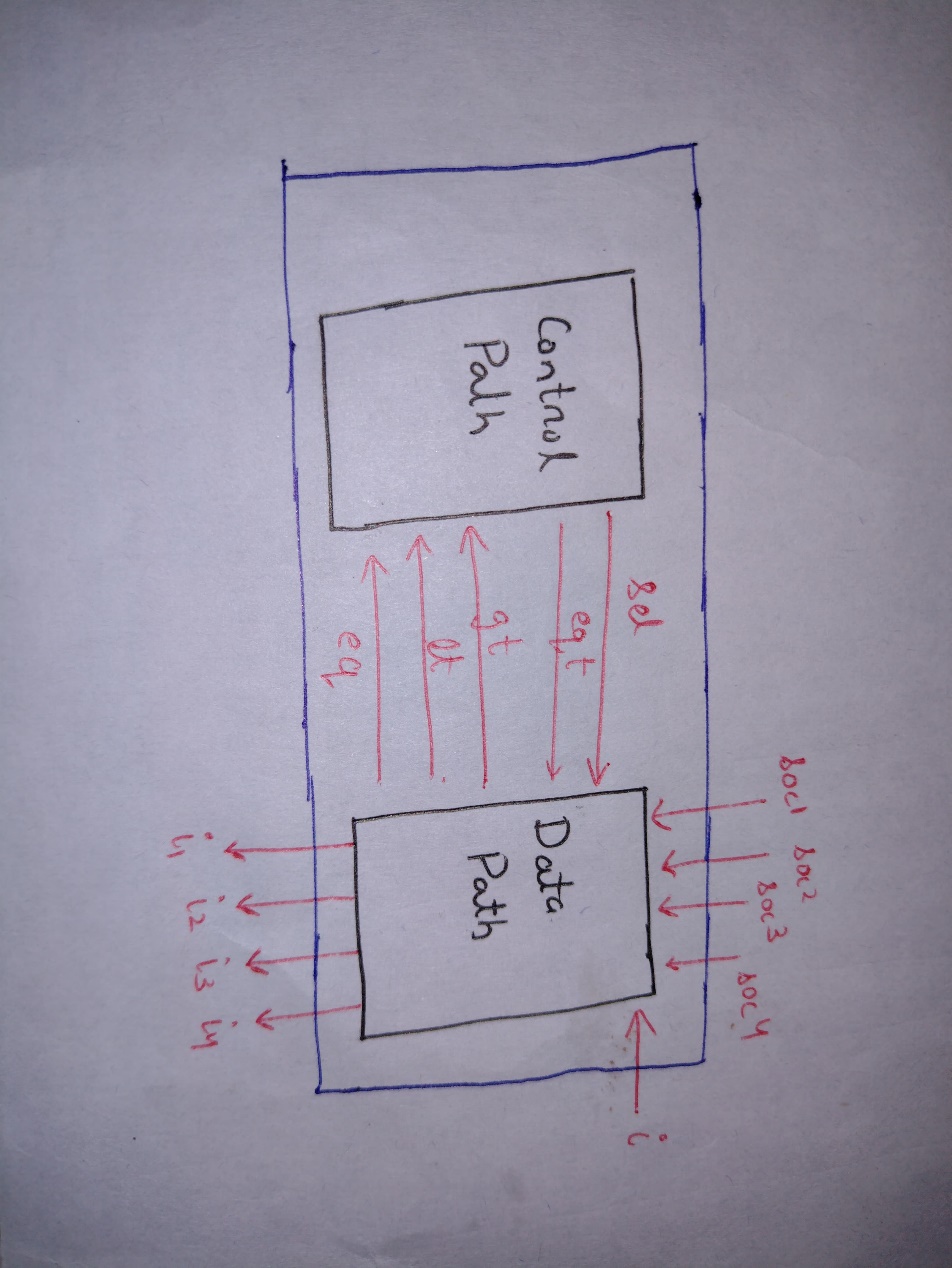
**Data Path**

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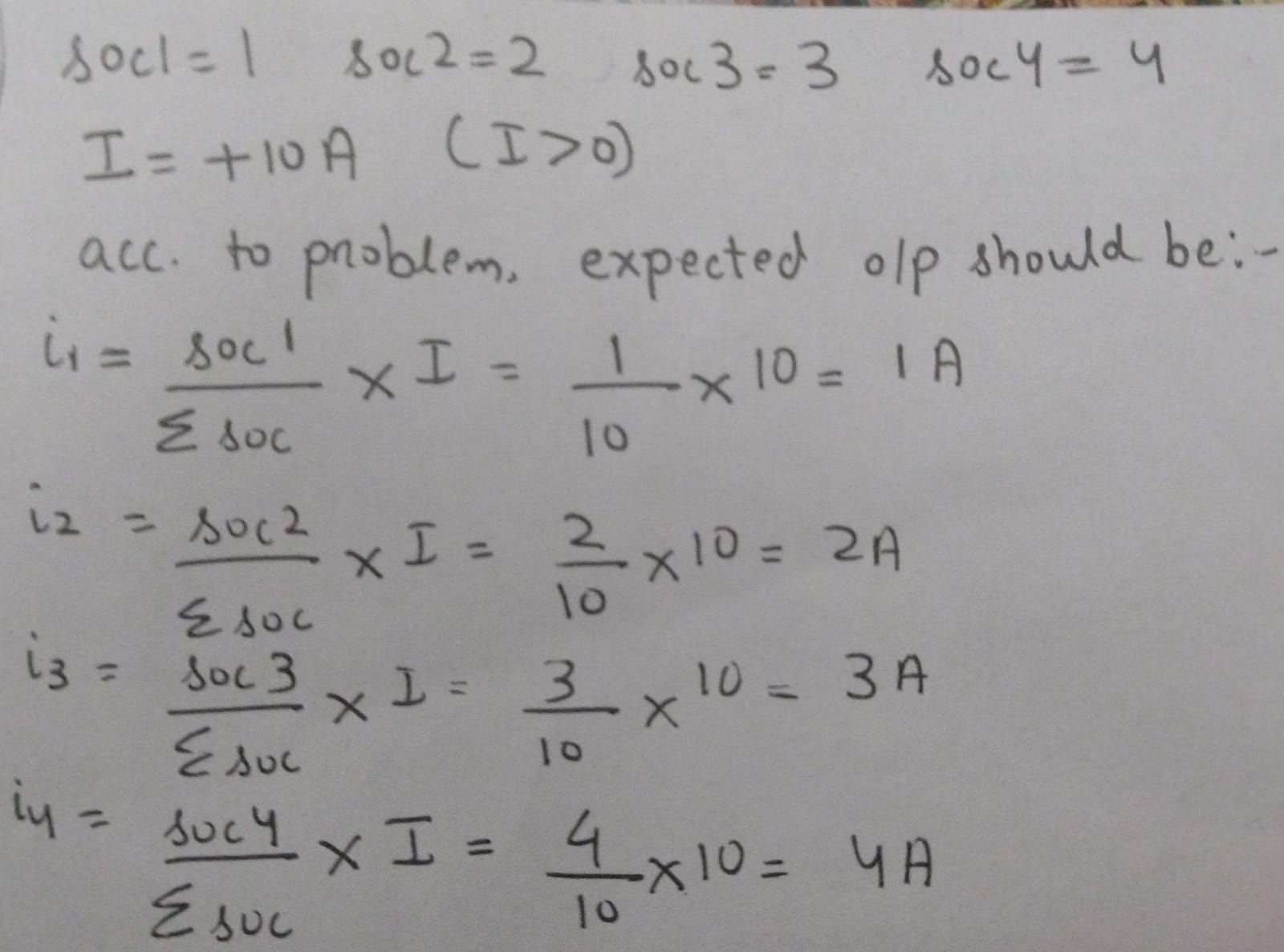
**Control Path**

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**Connecting DataPath and Control Path**

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**Testcase 1**

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**Output**

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Results are same, hence verified

**Testcase 2**

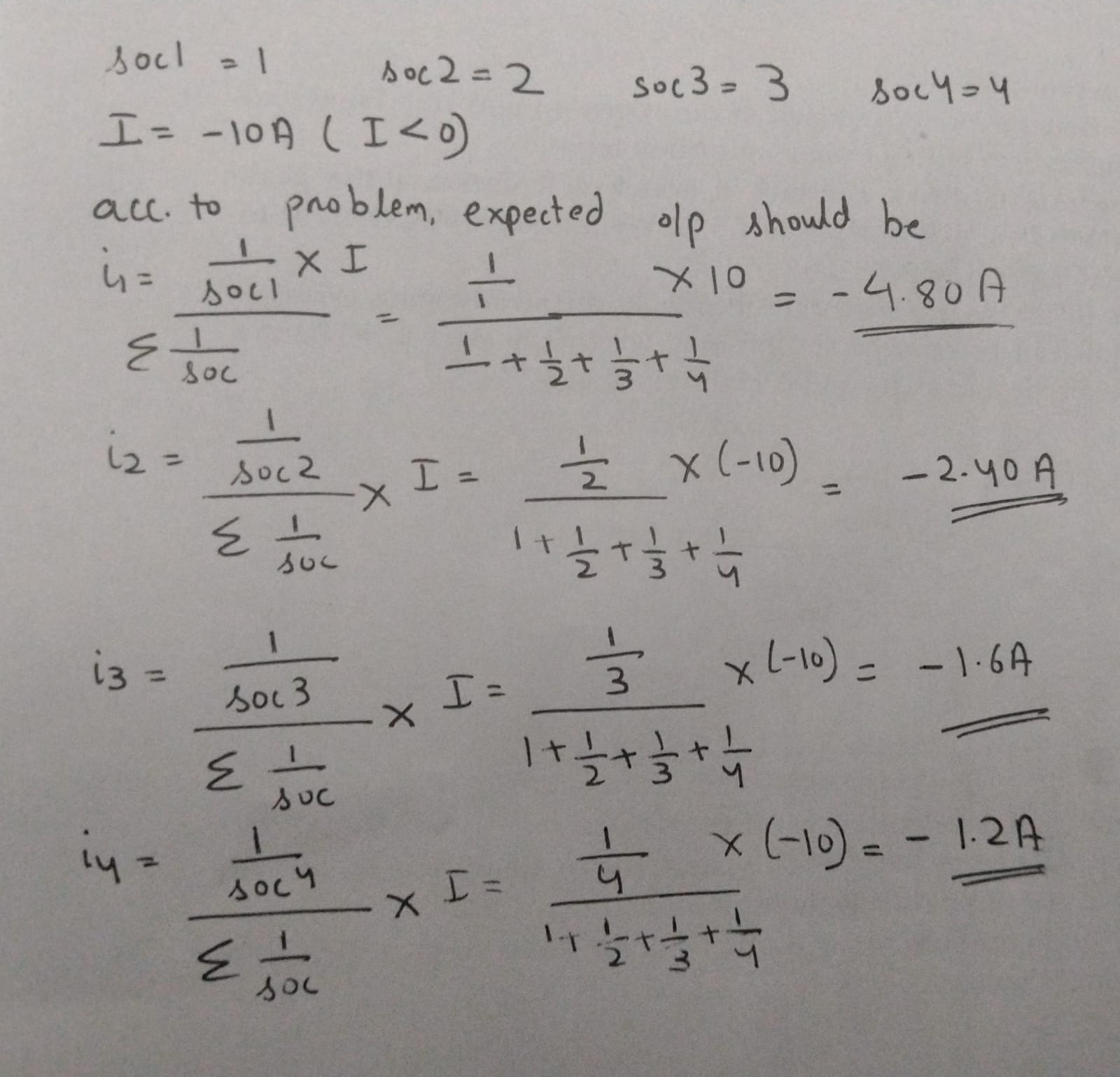
If I=0 expected values are I1=I2=I3=I4=0A

**Output**

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Results are same, hence verified

**Testcase 3**

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**Output**

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Results are same, hence verified